

1/11

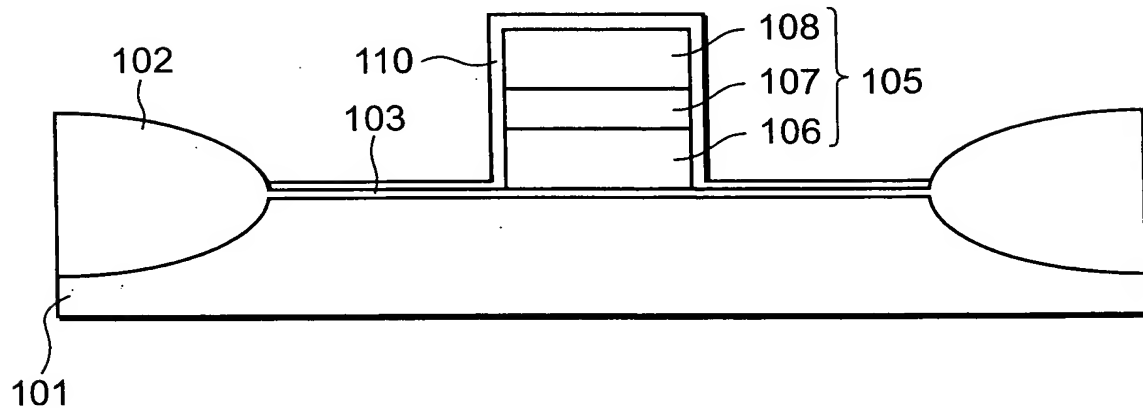


FIG. 1

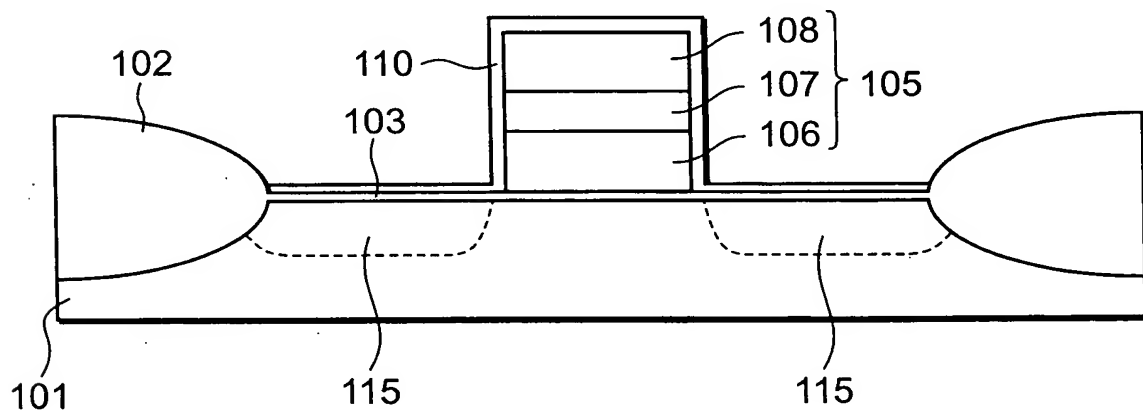


FIG. 2

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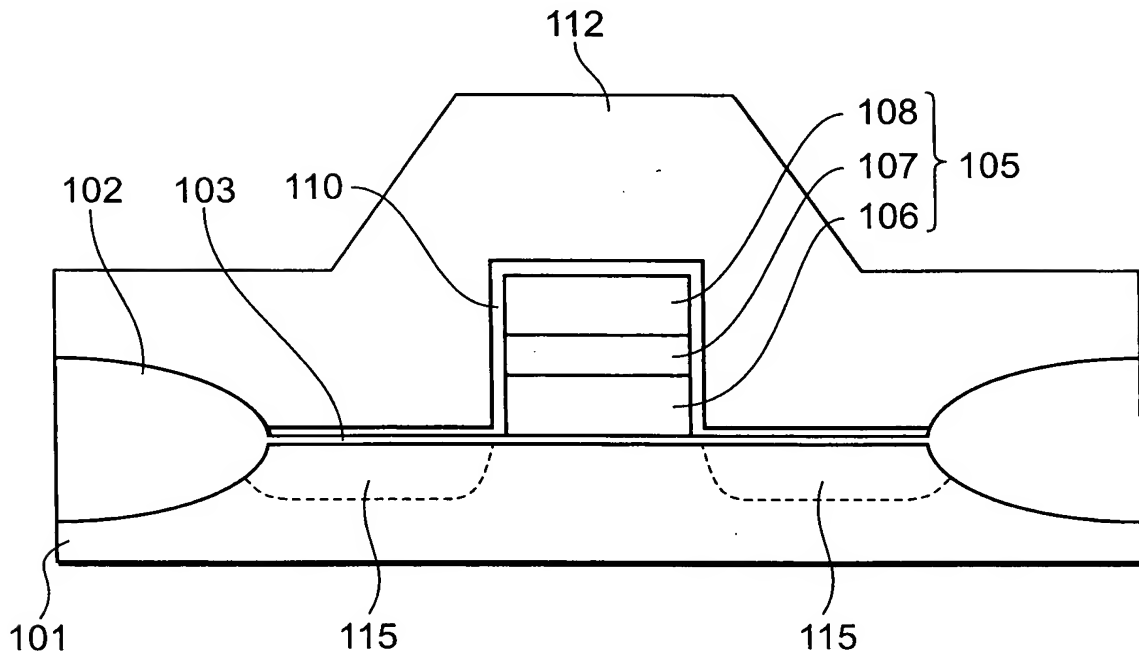


FIG. 3

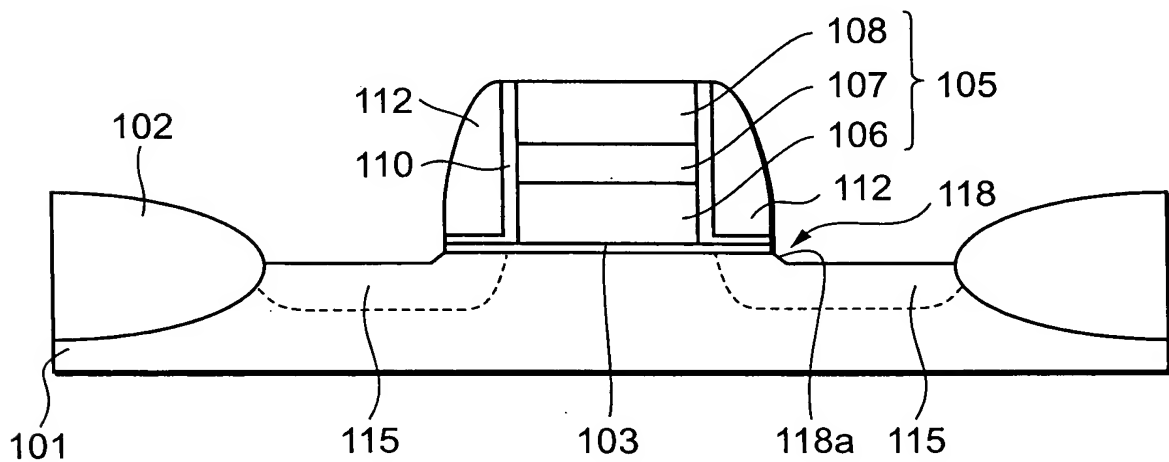


FIG. 4

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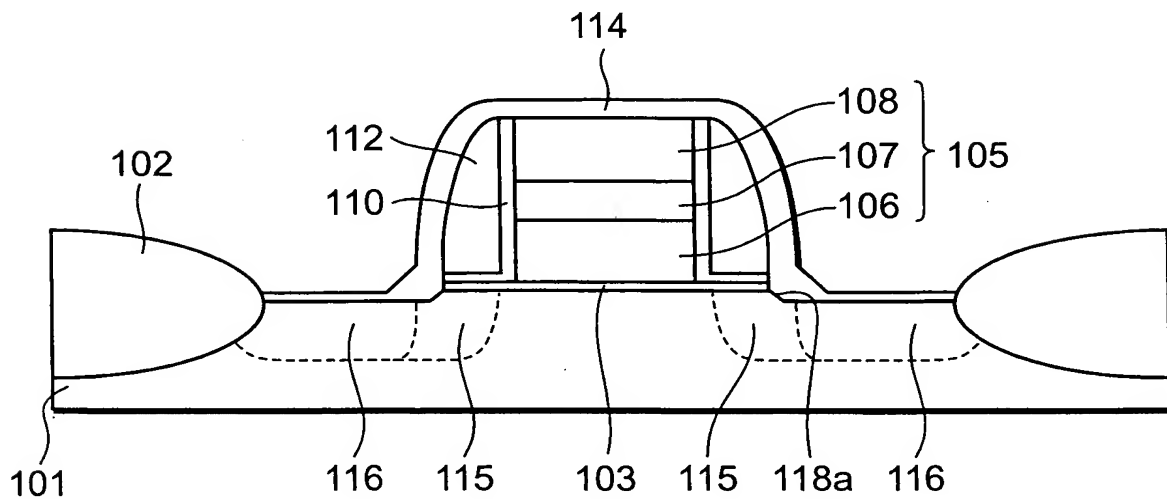


FIG. 5

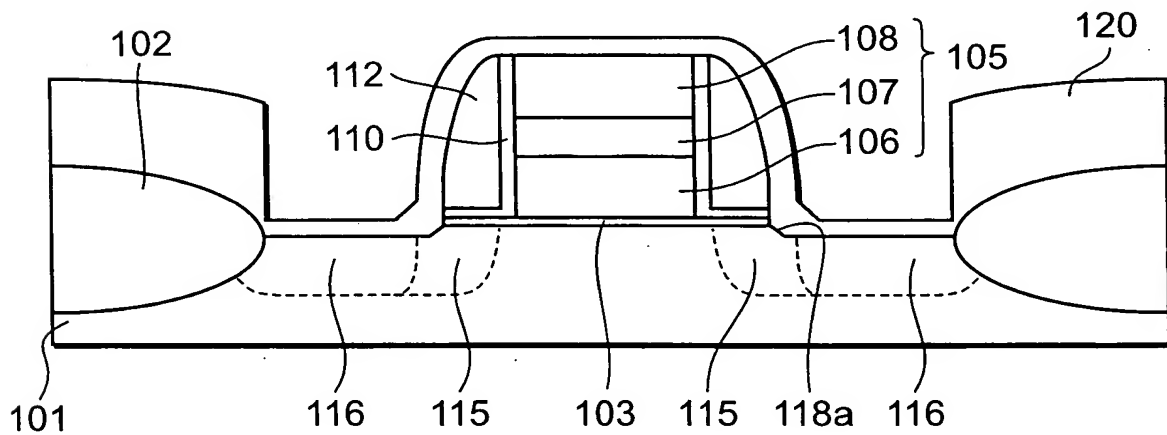


FIG. 6

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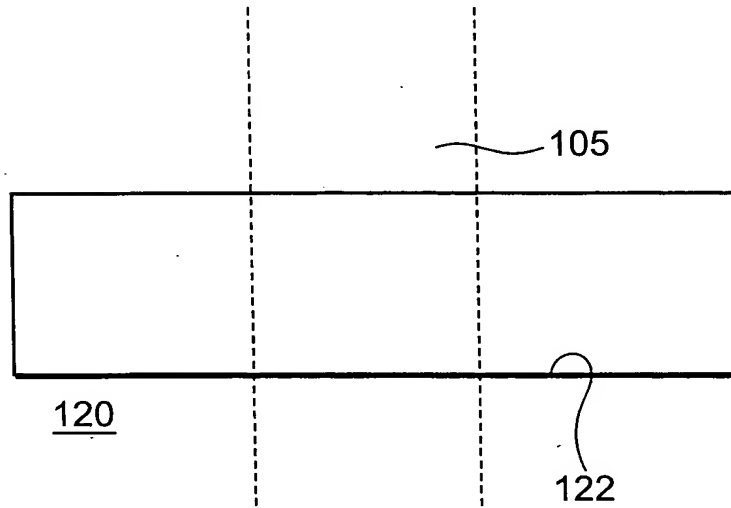


FIG. 7

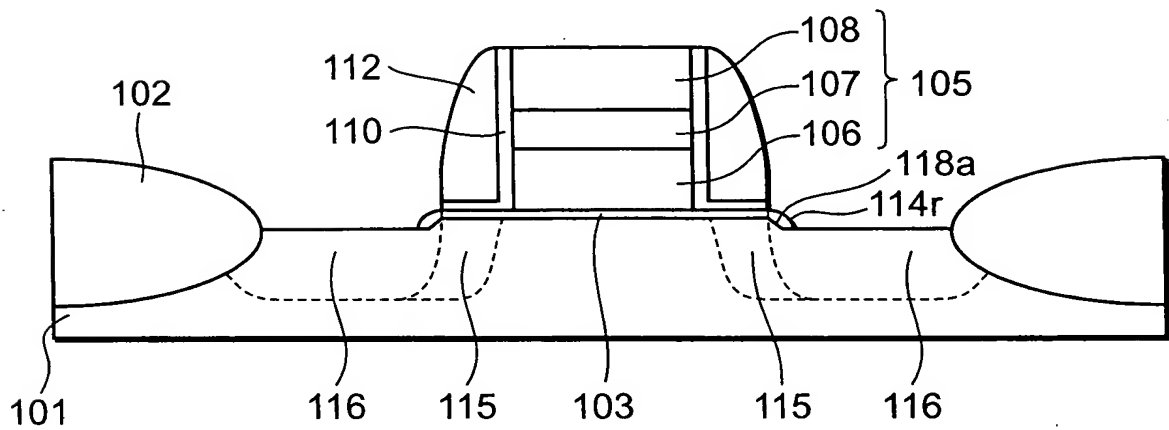


FIG. 8



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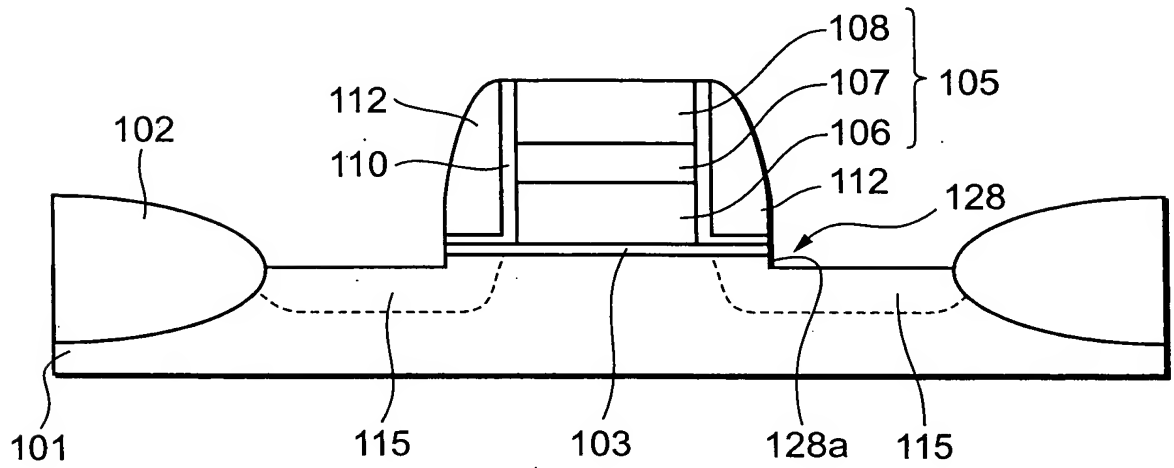


FIG. 11

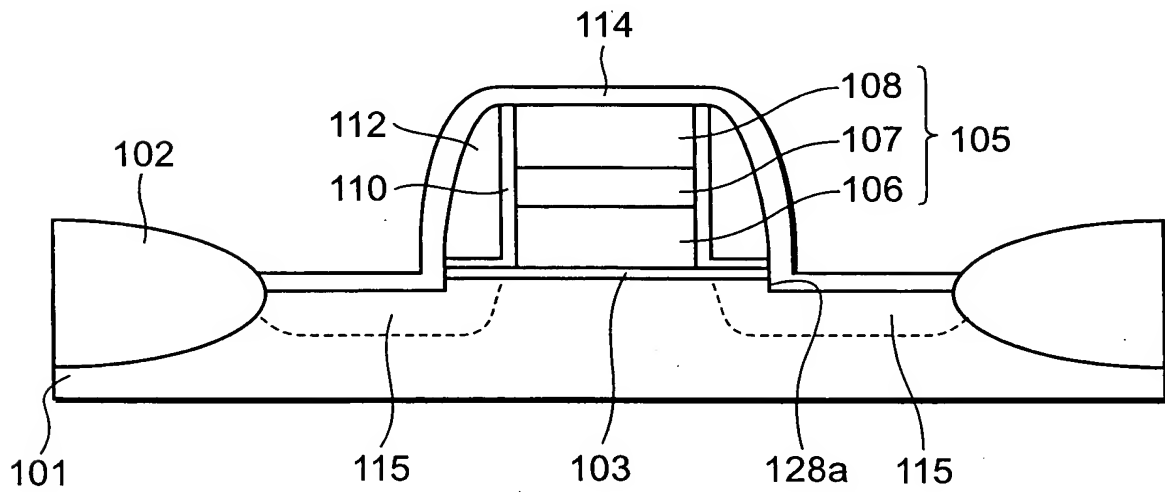


FIG. 12

This diagram shows a cross-sectional view of a semiconductor device. A central core structure is positioned on a substrate 101. The core includes a top layer 126, a middle section 110, and side walls 112. The middle section 110 is divided into horizontal layers 106, 107, and 108. The side walls 112 are connected to a base layer 115. The base layer 115 is further divided into regions 116 and 115. The core is flanked by side regions 124, which are connected to the base layer 115. The side regions 124 are further divided into regions 128a and 128b. A dimension  $D_s$  is indicated at the bottom, representing the width of the central core structure.

FIG. 14

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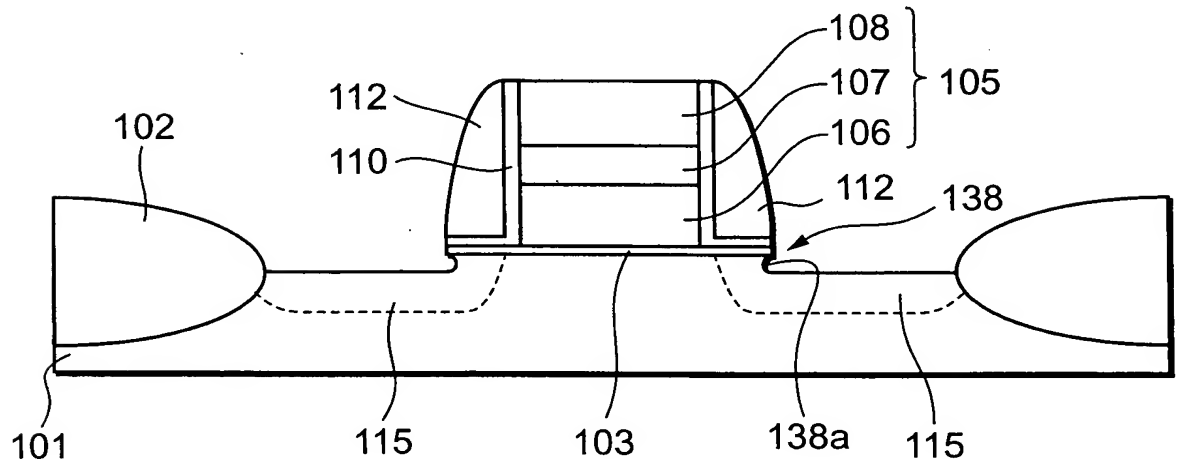


FIG. 15

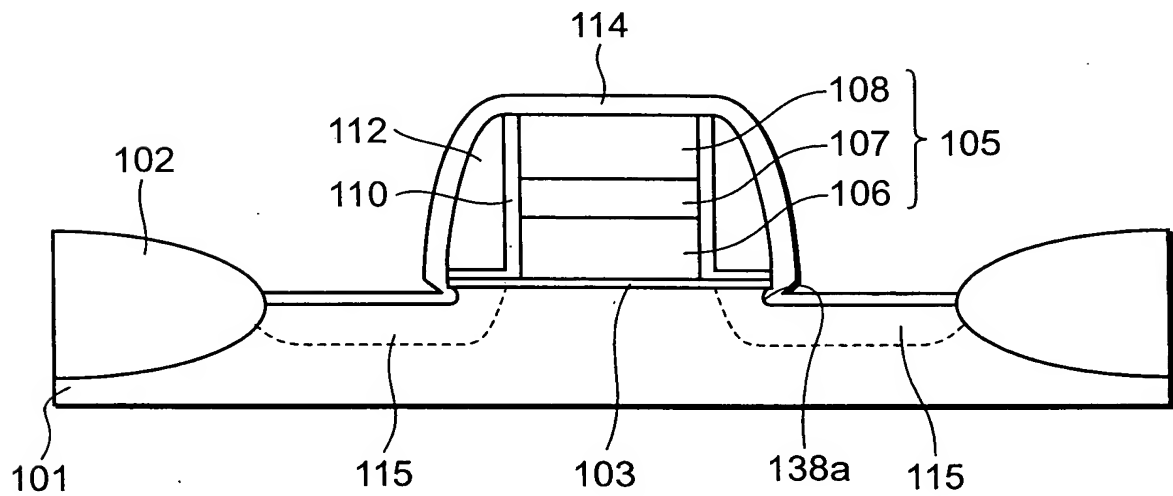


FIG. 16



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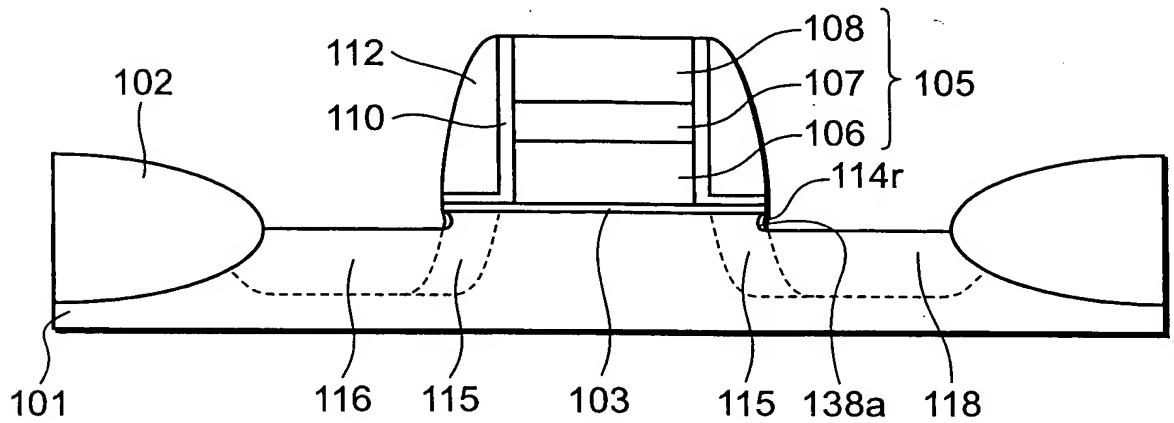


FIG. 17

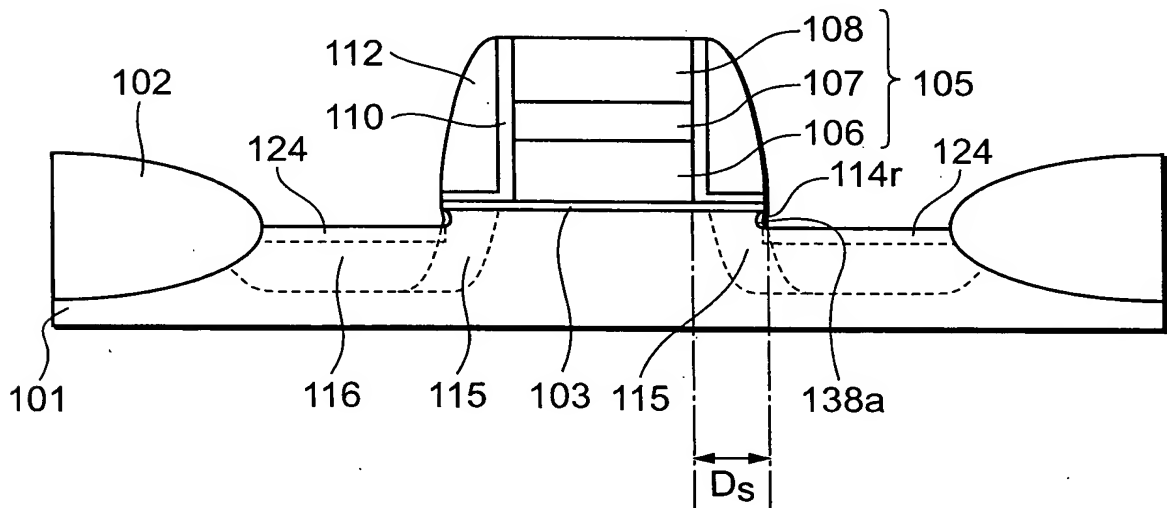


FIG. 18(a)

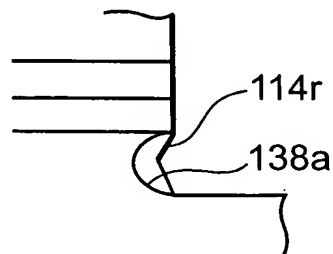


FIG. 18(b)

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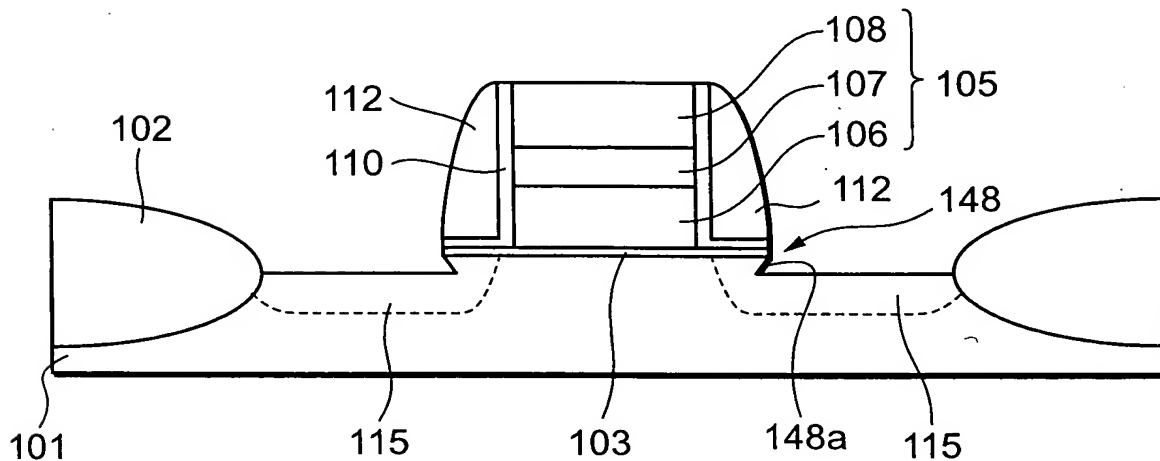


FIG. 19

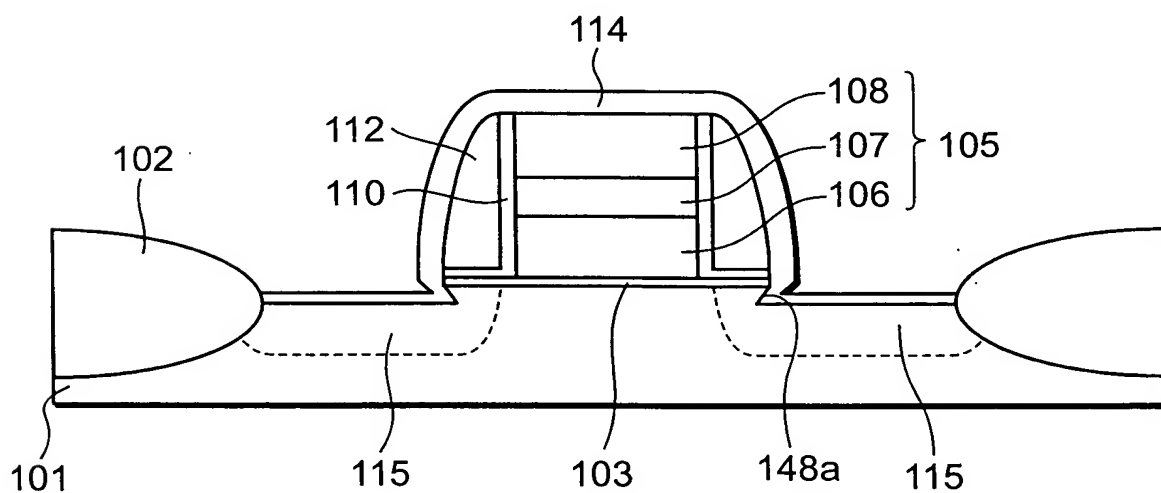


FIG. 20

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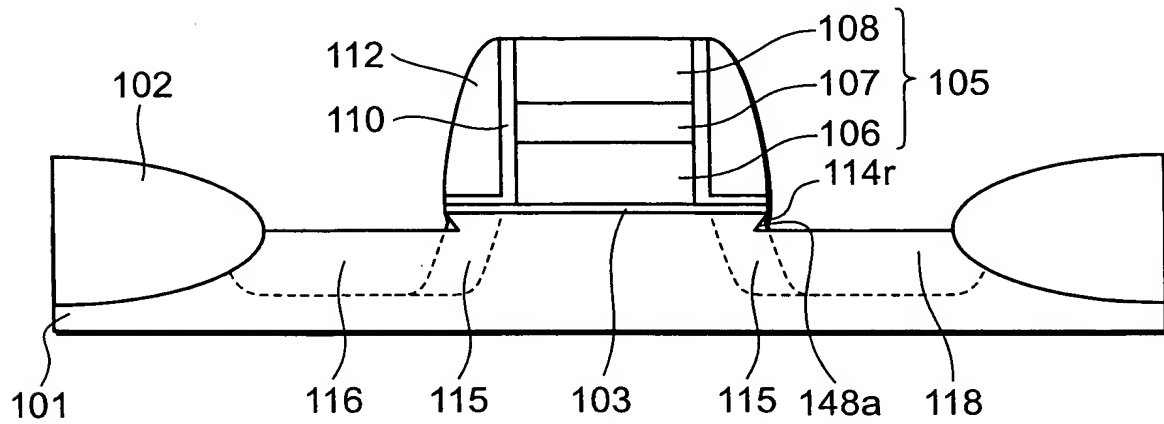


FIG. 21

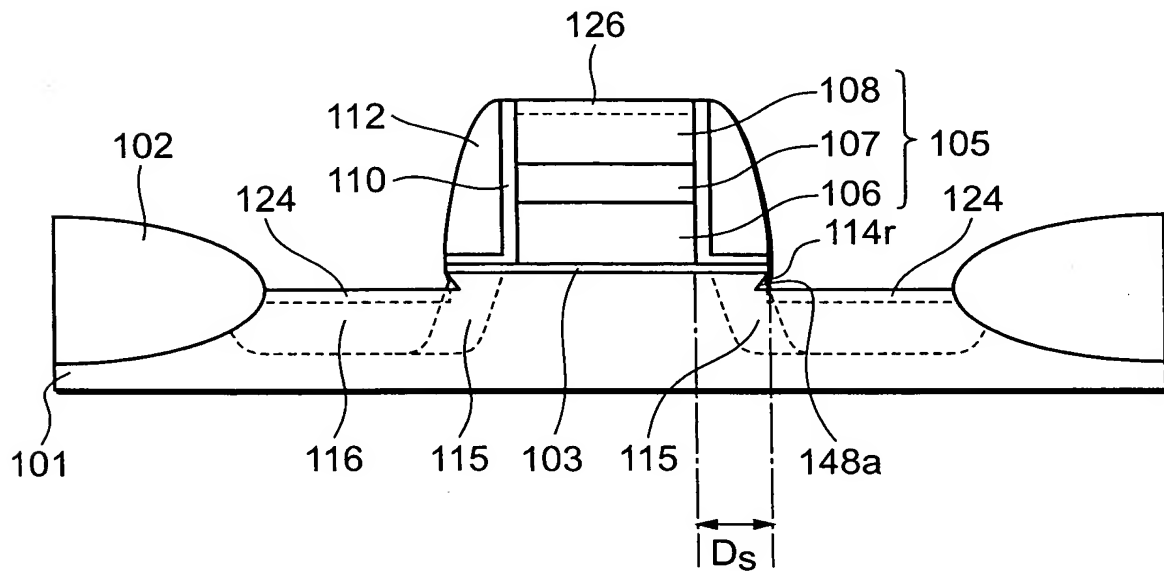


FIG. 22(a)

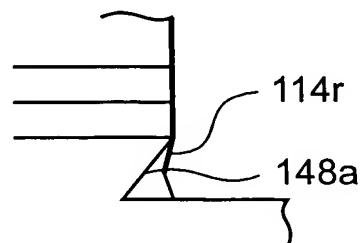


FIG. 22(b)